Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1-30 (Canceled)

31. (Currently amended) A NAND flash memory comprising:

a NAND memory cell array having a NAND block which comprises NAND memory cells;

first and second signal lines arranged in the NAND block with a first interval, connected to the NAND memory cells; and

third and fourth signal lines arranged with a second interval wider than the first interval; wherein

the first interval is a minimum interval less than 0.12 μm, and a maximum value of a voltage generated between the third and fourth signal lines is greater than a maximum value of a voltage generated between the first and second signal lines.

32. (Currently amended) The NAND flash memory according to claim 31, wherein the second signal line is connected to a first contact plug having the width larger than that of the second signal line, and the distance between the first signal line and the first contact plug is narrower than the first interval.

33. (Currently amended) The NAND flash memory according to claim 32, wherein the fourth signal line is connected to a second contact plug having the width larger than that of the fourth signal line, and the distance between the third signal line and the second contact plug is narrower than the second interval.

34. (Currently amended) The NAND flash memory according to claim 31, wherein the first and second signal line and the third and fourth signal lines are formed on the same wiring layer.

35. (Currently amended) The NAND flash memory according to claim 31, wherein the first and second signal line and the third and fourth signal lines are formed on a different wiring layer.

36. (Currently amended) The NAND flash memory according to claim 31, wherein the first and second signal lines are word lines.

37. (Currently amended) The NAND flash memory according to claim 31, wherein the first and second signal lines are bit lines.

38. (Currently amended) The NAND flash memory according to claim 31, wherein when the first interval is assumed to be S1, the maximum value of the voltage generated between the first and second signal lines is assumed to be V1 and the maximum value of the voltage generated between the third and fourth signal lines is assumed to be V2, the second interval S2 is expressed by $S2 = (V2/V1) \times S1$.

39. (Currently amended) The NAND flash memory according to claim 33, wherein when the distance between the first signal line and the first contact plug is assumed to be Sa, the maximum value of the voltage generated between the first and second signal lines is assumed to be V1 and the maximum value of the voltage generated between the third and fourth signal lines is assumed to be V2, the distance Sb between the third signal line and the second contact plug is expressed by $Sb = (V2/V1) \times Sa$.

40. (Currently amended) The NAND flash memory according to claim 31, wherein when a power supply potential is assumed to be Vcc, a ground potential is assumed to be Vss, an erase potential is assumed to be Vera and a forward bias voltage between a well area and a diffusion layer is assumed to be Vf, the maximum value Vmax1 of the voltage generated between the first and second signal lines is expressed by Vmax1 = Vcc-Vss and the maximum value Vmax2 of the voltage generated between the third and fourth signal lines is expressed by Vmax2 = (Vera-Vf) -Vcc.

41. (Currently amended) A NAND flash memory comprising:

a NAND memory cell array having a NAND block which comprises NAND memory cells;

first and second signal lines arranged in the NAND block with a first interval, connected to the NAND memory cells;

a third signal line, wherein a second interval between the first and third signal lines is wider than the first interval; and

a first transistor configured to connect the second and third signal lines; wherein

the first interval is a minimum interval less than 0.12 μm, and a maximum value of a voltage generated between the first and third signal lines is greater than a maximum value of a voltage generated between the first and second signal lines.

42. (Currently amended) The NAND flash memory according to claim 41, wherein the second signal line is connected to the first transistor through the wiring layer formed just under the second signal line, and the third signal line is connected to the first transistor through the wiring layer formed just under the third signal line.

43. (Currently amended) The NAND flash memory according to claim 41, wherein the first and second signal lines are word lines.

44. (Currently amended) The NAND flash memory according to claim 41, wherein the first and second signal lines are bit lines.

45. (Currently amended) The NAND flash memory according to claim 41, wherein the third signal line is a line to give a predetermined potential to the second signal line, during read operation.

46. (Currently amended) The NAND flash memory according to claim 41, wherein the third signal line is a line to connect the second signal line to a sense amplifier.

47. (Currently amended) The NAND flash memory according to claim 41, wherein the transistor turns off, each of the first and second signal lines has an

erase potential and the third signal line has a power supply potential, during erase operation.

48. (Currently amended) The NAND flash memory according to claim 41, wherein when the first interval is assumed to be S1, the maximum value of the voltage generated between the first and second signal lines is assumed to be V1 and the maximum value of the voltage generated between the first and third signal lines is assumed to be V2, the second interval S2 is expressed by $S2 = (V2/V1) \times S1$.

49. (Currently amended) The NAND flash memory according to claim 41, wherein when a power supply potential is assumed to be Vcc, a ground potential is assumed to be Vss, an erase potential is assumed to be Vera and a forward bias voltage between a well area and a diffusion layer is assumed to be Vf, the maximum value Vmax1 of the voltage generated between the first and second signal lines is expressed by Vmax1 = Vcc-Vss and the maximum value Vmax2 of the voltage generated between the first and third signal lines is expressed by Vmax2 = (Vera-Vf) -Vcc.

50. (Currently amended) The NAND flash memory according to claim 41, wherein the second signal line is connected to a first contact plug having the width larger than that of the second signal line, and the distance between the first signal line and the first contact plug is narrower than the first interval.

51. (Currently amended) The NAND flash memory according to claim 50, wherein the third signal line is connected to a second contact plug having the width larger than that of the third signal line, and the distance between the first signal line and the second contact plug is narrower than the second interval.

52. (Currently amended) The NAND flash memory according to claim 51, wherein when the distance between the first signal line and the first contact plug is assumed to be Sa, the maximum value of the voltage generated between the first and second signal lines is assumed to be V1 and the maximum value of the voltage generated between the first and third signal lines is assumed to be V2, the distance

Sb between the first signal line and the second contact plug is expressed by Sb = (V2/V1) × Sa.

53. (Currently amended) The NAND flash memory according to claim 41, further comprising a second transistor connected to the first signal line; wherein

the first and second transistors are arranged in being adjacent in the extending direction of the first and second signal lines.

54. (Currently amended) The NAND flash memory according to claim 53, wherein the second transistor is connected to between the first and third signal lines.

55. (Currently amended) A NAND flash memory comprising:

a NAND memory cell array having a NAND block which comprises NAND memory cells;

first and second signal lines arranged in the NAND block with a first interval, connected to the NAND memory cells;

a third signal line; and

a first transistor configured to connect the second and third signal lines; wherein

the first interval is a minimum interval less than 0.12 μm, and a maximum value of a voltage generated between the first and third signal lines is greater than a maximum value of a voltage generated between the first and second signal lines, and the third signal line is arranged at a position not adjacent to the first signal line.

56. (Currently amended) The NAND flash memory according to claim 55, wherein the second signal line is connected to the first transistor through the wiring layer formed just under the second signal line, and the third signal line is connected to the first transistor through the wiring layer formed just under the third signal line.

57. (Currently amended) The NAND flash memory according to claim 55, wherein the first and second signal lines are word lines.

58. (Currently amended) The NAND flash memory according to claim 55, wherein the first and second signal lines are bit lines.

59. (Currently amended) The NAND flash memory according to claim 55, wherein the third signal line is a line to give a predetermined potential to the second signal line, during read operation.

60. (Currently amended) The NAND flash memory according to claim 55, wherein the third signal line is a line to connect the second signal line to a sense amplifier.

61. (Currently amended) The NAND flash memory according to claim 55, wherein the transistor turns off, each of the first and second signal lines has an erase potential and the third signal line has a power supply potential, during erase operation.

62. (Currently amended) The NAND flash memory according to claim 55, further comprising a fourth signal line arranged in being adjacent to at least one of the first, second and third signal lines; wherein

the fourth signal line is a dummy line set to be floated its potential.